ABSTRACT OF THE DISCLOSURE

A bus controller including a processing means for performing processings of levels having cycle numbers which are different dependent on requesters which respectively issue an access request to a common memory. When it is expected from the present cycle number that a limit cycle number is exceeded, the bus controller selects a processing level with which the processing is performed with a smaller cycle number, or performs a control of giving no permission to a non-realtime bus access request. Thereby, it is enabled to design a system with a cycle number that is smaller than the total sum of the maximum access cycle numbers multiplied by the maximum access times over all requesters.